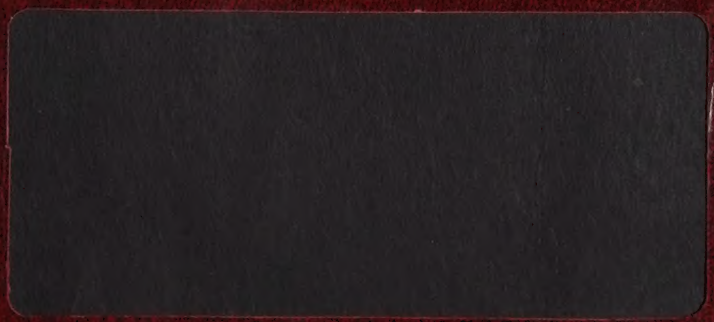
Instruction manual



DATA I/O

Programming systems for tomorrow...today

PROM PROGRAMMER
PROGRAM CARD SET
909/919-1512

025-1512 REV A FEB 79

TABLE OF CONTENTS

SECTION 1. SPECIFICATIONS

1.1 INTRODUCTION 1-1

1.2 PROGRAMMING ALGORITHM 1-1

1.3 CALIBRATOR PROGRAM ADAPTER 1-1

1.4 CALIBRATION REQUIREMENTS 1-1

SECTION 2. INSTALLATION

2.1 DIGITAL CARD JUMPERS 2-1

2.2 CARD SET INSERTION 2-1
- 2.2.1 Models 1–5 2-1
- 2.2.2 Models 7 and 9 2-1
- 2.2.3 Systems 17 and 19. 2-2

SECTION 3. OPERATION

3.1 OPERATION 3-1

SECTION 4. CALIBRATION

4.1 INTRODUCTION 4-1

4.2 TEST SET-UP. 4-1
- 4.2.1 Models 1 - 5 4-1
- 4.2.2 Model 9. 4-1
- 4.2.3 System 19 4-3

4.3 PROCEDURES FOR CALIBRATION. 4-3
- 4.3.1 Check the State of the Start/Stop Line 4-5
- 4.3.2 Set the State of the Start/Stop Line 4-5
- 4.3.3 Set the State of the FWD/REV Line 4-5
- 4.3.4 Load Data onto the DI Bus 4-5
- 4.3.5 Confirm Data on the DO Bus 4-6

4.4 WAVEFORM OBSERVATION 4-6
- 4.4.1 Calibration Equipment Set-up 4-6
- 4.4.2 Test Procedure 4-8
- 4.4.3 Reject Jumper Reinstallation and Abort Test 4-9

SECTION 5. CIRCUIT DESCRIPTION

5.1 INTRODUCTION 5-1
5.1.1 Digital Card 5-1
5.1.2 Analog Card 5-1
5.1.3 Detailed Circuit Description 5-1

5.2 DIGITAL CARD 5-2
5.2.1 Block Diagram 5-2
5.2.2 Select and Mode Control 5-2
5.2.3 Master Clock 5-2
5.2.4 Timing Generator 5-2
5.2.5 Read Operation 5-2
5.2.6 Program Operation 5-3
5.2.7 Overprogram Operation 5-3
5.2.8 Word Limit 5-3
5.2.9 4/8 Bit Mode 5-3

5.3 ANALOG CARD 5-3
5.3.1 Block Diagram 5-3
5.3.2 VCC Generator 5-4
5.3.3 Program Voltage Generator (VPP) 5-4
5.3.4 Data Bus Drivers 5-4
5.3.5 Comparator and Data Out Drivers 5-4
5.3.6 Chip Enable and PD/PGM Buffers 5-4

LIST OF FIGURES

1-1 Parts included in the a)Programming Pak and b)Program Card Set
2-1 Digital Card Jumper Locations
2-2 Installation of Card Set in Model 3 or 5
2-3 Installation of Card Set in Model 7 or 9
2-4 Installation of the Program Card Set in the Programming Pak
4-1 Set-up of Models 1-5 for DC Calibration
4-2 Set-up of Model 9 for DC Calibration
4-3 Set-up of System 19 for DC Calibration
4-4 Analog Card Adjustment Locations
4-5 Calibrator Set-up for Waveform Observations
5-1 Simplified Block Diagram of Program Card Set
5-2 Block Diagram, 1348 Digital Program Card
5-3 Block Diagram, 1512 Analog Card

LIST OF TABLES

1-1 Applications of the Program Card Set
2-1 Customer-Selectable Digital Card Jumpers

SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
INTEL				
2048x8 MOS	2716/8716	VOL TS	24 PIN	1510
4096x8 MOS	2732	VOL TS	24 PIN	1531
1024x8 MOS	2758	VOL TS	24 PIN	1366-3
1024x8 MOS	2758 S 1865	VOL TS	24 PIN	1366-4
	2732A			1620
MOSTEK				
2048x8 MOS	2716	VOL TS	24 PIN	1510
TEXAS INSTRUMENTS				
2048x8 MOS	2516	VOL TS	24 PIN	1510
4096x8 MOS	2532	VOL TS	24 PIN	1511
TOSHIBA				
2048x8 MOS	323	VOL TS	24 PIN	1510

The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences of these waveforms.

A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909- part number. See Figure 1-1 b).

1.2 PROGRAMMING ALGORITHM

The 909-1512 Program Card Set is designed to program data at each address successfully before advancing to the next address. A single program pulse is applied to the device at each address as data levels appear on the bit lines representing the specific pattern to be programmed (parallel programming).

The Program Card Set also provides power and enable levels required for the duration of the program sequence. If any bit fails to program after a single attempt, the Program Card Set will abort the Program mode and halt machine operation (one pulse reject).

1.3 CALIBRATOR PROGRAM ADAPTER

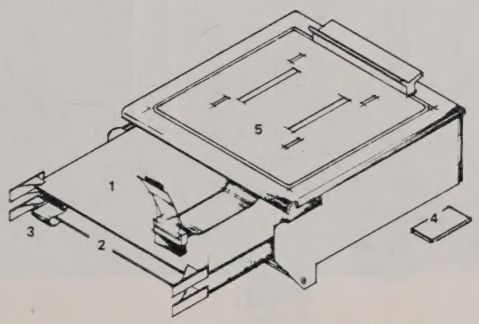
The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.

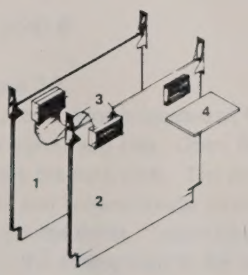
1.4 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1 - 9 Programmers

1. DIGITAL CARD	701-1348
2. ANALOG CARD	701-1512
3. INTERCONNECT CABLE	709-1608
4. CALIB. PROGRAM ADAPTER	910-1512
5. PROGRAMMING PAK CARRIER	940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

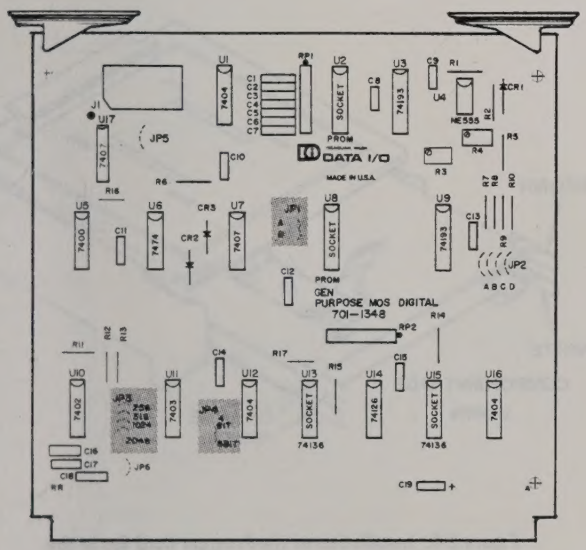


Figure 2-1. Digital Card Jumper Locations

Table 2-1. Customer - Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP1	Reject	A	
JP3	Word Limit Jumper	2048	Selection defaults to programmer and socket adapter
JP4	Word Width	8 bit	Selection defaults to socket adapter

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

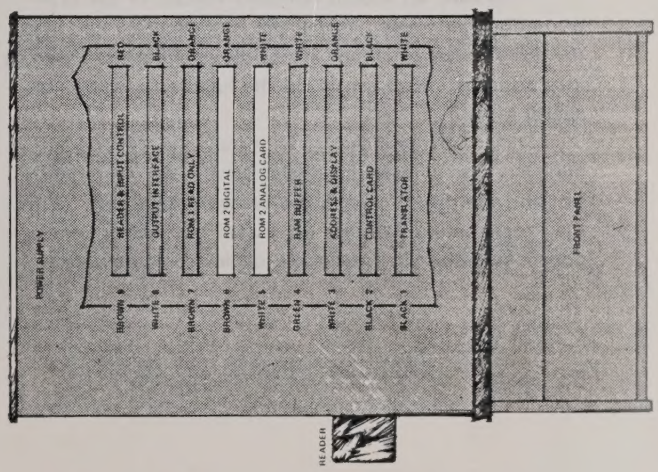


Figure 2-2. Installation of Card Set in Model 3 or 5

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down — the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

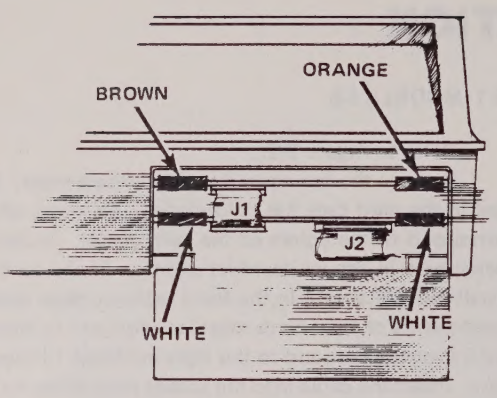


Figure 2-3. Installation of Card Set in Model 7 or 9

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

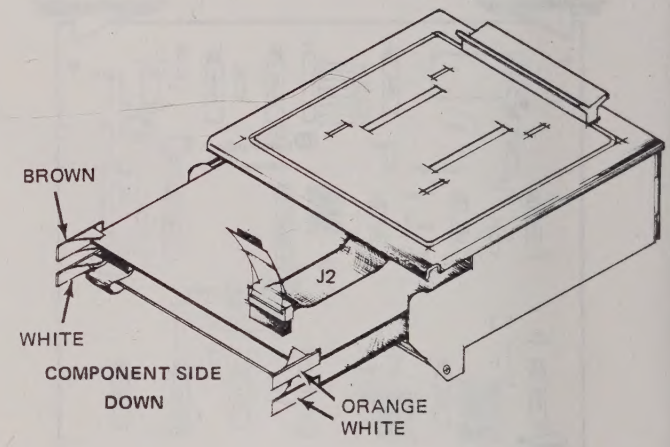


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

The Program Card Set provides the link between the device in the socket adapter and the programmer's memory and control electronics. Its functions are directly controlled by the programmer. Complete instructions for operations using the card set are in the programmer instruction manual.

SECTION 4

CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

1. Data I/O Universal Calibrator, P/N 910-1071
2. Calibrator Extender Fixture:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1520

3. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.
4. A potentiometer adjustment tool
5. Dual-trace oscilloscope — Tektronix 465 or equivalent
6. A jumper wire approximately 12 inches in length
7. Data I/O interconnection cables:
   Models 1-5: P/N 709-1613
   Model 9, System 19: P/N 709-2608, 709-1613.
8. Calibrator Program Adapter

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1 – 5

Refer to Figure 4-1.

1. Make sure the programmer power is OFF.
2. Remove the cover from the programmer and remove the Program Card Set from the card cage.
3. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the digital card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

4. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card in the digital card position (brown/orange) in the programmer card cage.
5. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.
6. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

7. Connect the DVM ground lead to the GND test point on the Universal Calibrator.
8. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

   RESET
   ROM2 – ROM2
   MANUAL
   PROGRAM
   START

4.2.2 MODEL 9

Refer to Figure 4-2.

1. Make sure the programmer power is OFF.
2. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

Figure 4-1. Set-up of Models 1-5 for DC Calibration

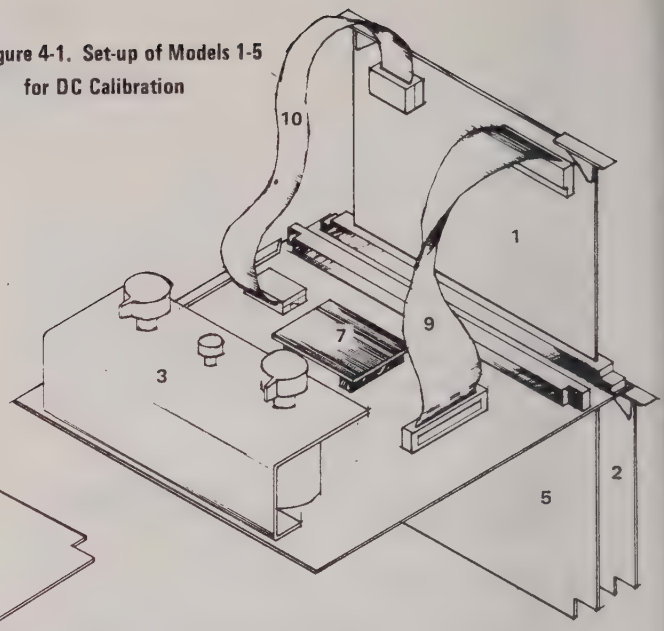
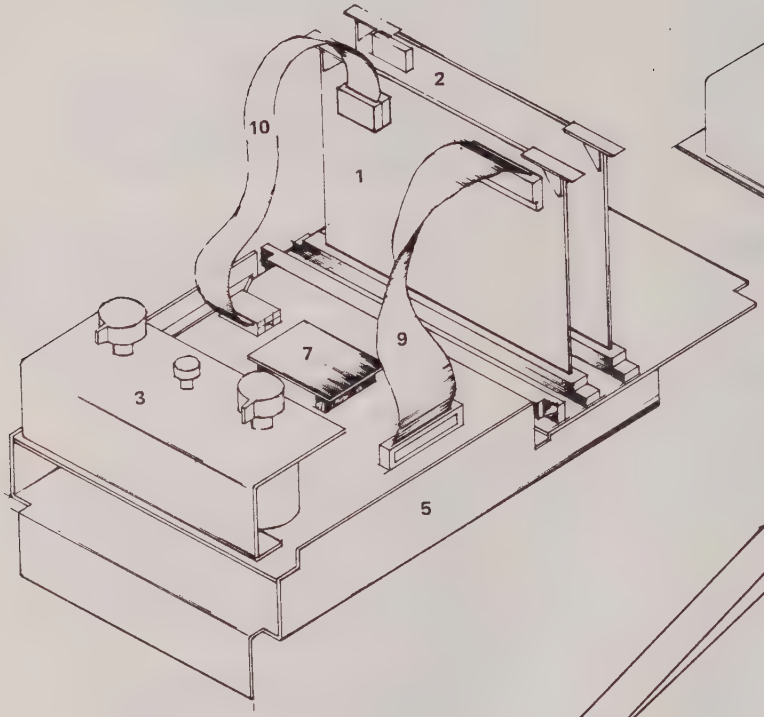


Figure 4-2. Set-up of Model 9 for DC Calibration



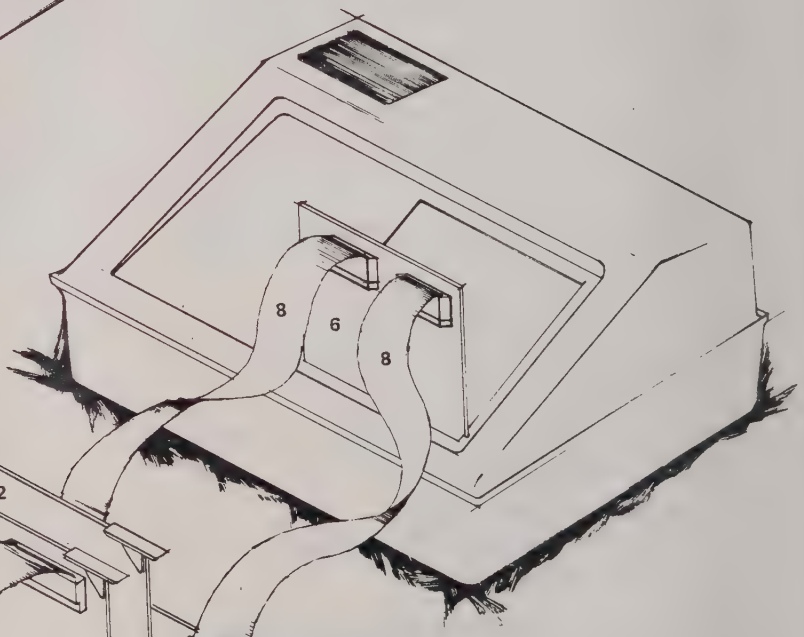
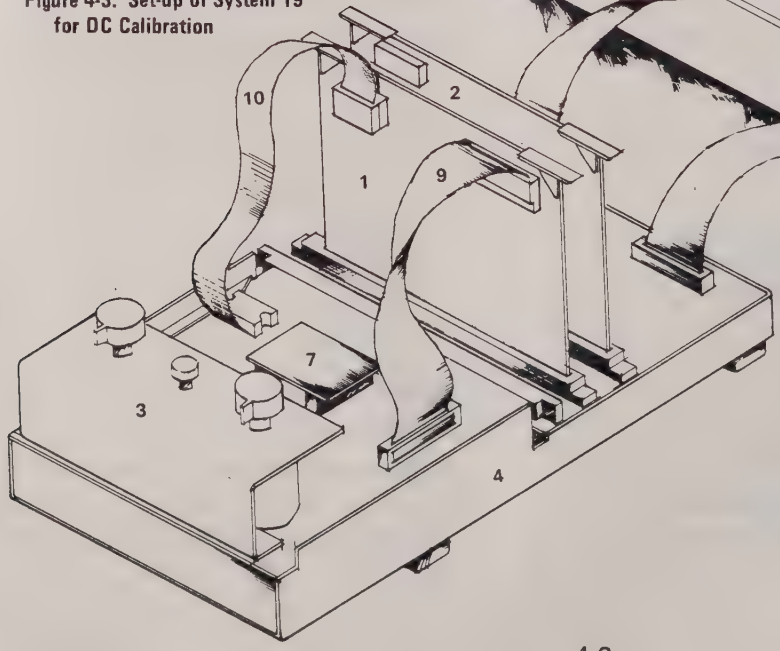


Figure 4-3. Set-up of System 19 for DC Calibration



1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATOR EXTENDER
5. CALIBRATOR EXTENDER FIXTURE
6. CALIBRATOR INTERFACE
7. CALIBRATOR PROGRAM ADAPTER
8. 50-CONDUCTOR CABLE
9. 26-CONDUCTOR CABLE
10. 16-CONDUCTOR CABLE

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

3. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the digital card.

4. Install the Extender Card, P/N 910-1074, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card into the digital card position (brown/orange) in the programmer card cage.

5. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

6. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

7. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

8. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

   EXECUTE

   NORMAL/INVERT switch to INVERT

4.2.3 SYSTEM 19

Refer to Figure 4-3.

1. Make sure the programmer is OFF.

2. Remove the Programming Pak from the programmer.

3. Insert the Calibrator Interface, P/N 702-1538, into the Programming Pak port.

4. Connect the two 50-pin cables, P/N 709-2700, to the Calibrator Interface card. Be sure the cables are oriented properly: the red stripes must align with the connector dots.

5. Connect the free ends of the 50-pin cables to the Universal Calibrator/Calibrator Extender Fixture. Be sure the cables are oriented with the red stripes and connector dots aligned.

6. Remove the card set to be calibrated from its Programming Pak by disconnecting J2 of the analog card from the Programming Pak socket receptacle PC board.

7. Install the card set in the two blue card slots on the Calibrator Extender. The analog card should be in front with the component sides of both boards facing the Universal Calibrator.

8. Connect the 26-conductor cable from J2 of the analog card to J2 of the Universal Calibrator, making sure to align the red stripe to the connector dot.

9. Disconnect the 16-conductor cable from J1 on the digital card and route it to J1 on the Universal Calibrator, making sure to align the red stripe to the connector dot.

10. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number of the Calibrator Program Adapter corresponds to the 909-XXXX part number of the Program Card Set.

11. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

12. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

    SELECT
    C1
    START

    The TEST light will come ON.

4.3 PROCEDURES FOR CALIBRATION

The Calibration Chart, between pages 4-4 and 4-5, gives the steps for complete DC calibration. It is to be used only with the Calibrator Program Adapter specified in the title block of the chart.

The first five steps on the Calibration Chart cover the level checks of the programmer power supplies. If any adjustment is necessary in these steps, refer to the Programmer Manual. The remaining steps provide information for calibration of the Program Card Set.

● The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

● The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance. Some steps, labeled Adjustment Steps, give a nominal (NOM) value and prescribe adjustment to that value if the level is out of the MIN-MAX range.

● The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer. The remaining entries in the ADJ column refer to potentiometers on the analog card. Refer to Figure 4-4 for locations of the potentiometers.

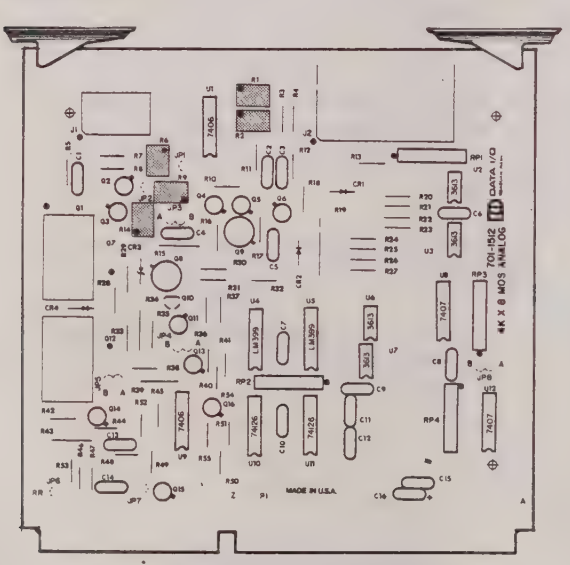


Figure 4-4. Analog Card Adjustment Locations

● The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the calibration chart may require changing of switch positions. With the proper S2 and S3 positions selected, press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

● The TEST POINT column gives test point locations for the DVM probe. Most test points are located on the Universal Calibrator; some points are located on the program card. For instance, if a test point is designated as U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

● The LIMITS column is divided into three portions: MIN (minimum), NOM (nominal), and MAX (maximum). The values given are in volts and indicate the range into which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the programmer (or Program Card Set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (in adjustment steps), the card is nonfunctional and should not be used for programming.

● The COMMENTS column on the right side of the chart provides information for certain calibration steps including call-outs of programmer operations required in some steps. The programmer provides signals to the card set on the Address bus, the Data Input bus, the START/STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set the following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4 3.1 – 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer to paragraphs 4.3.1 – 4.3.5 as necessary.

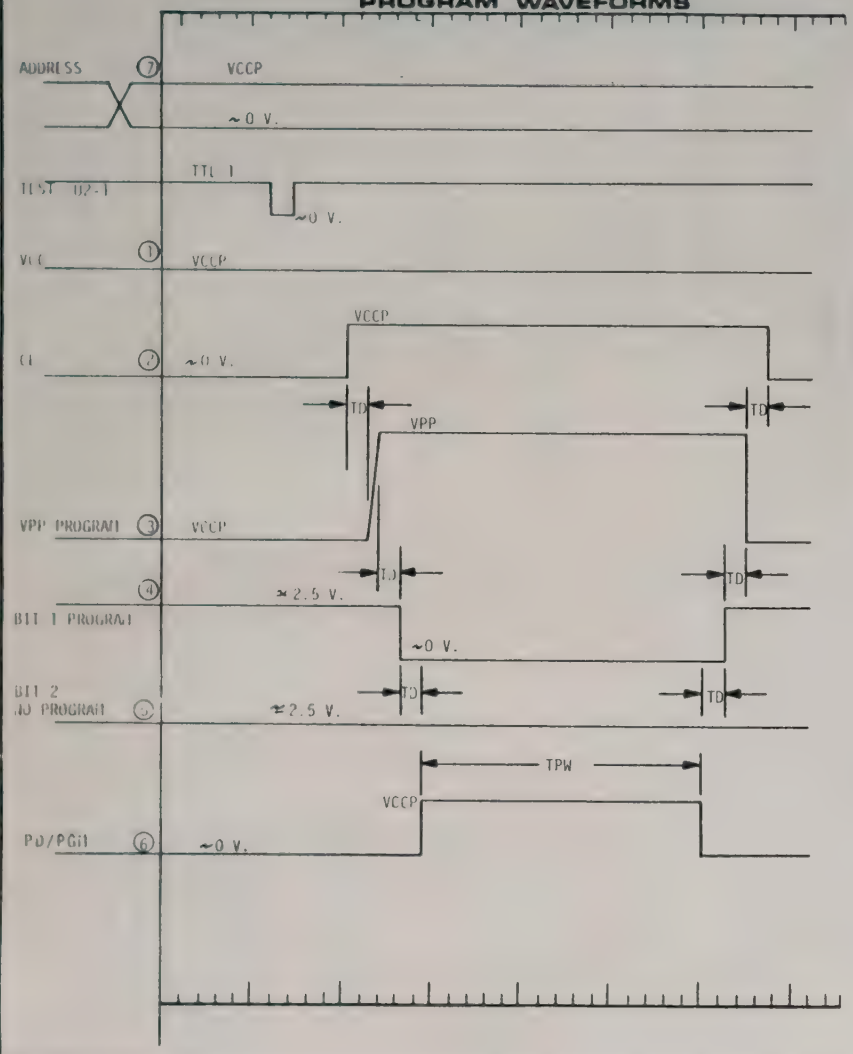
MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions of software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

DATE	SYM	REVISION RECORD	DR	CK
6-2-78	A	RELEASE	AB	
11-78	-	ECN #2594	FS	

PROGRAM WAVEFORMS



NOTES

DIGITAL CARD JUMPERS

JP1 = A=1 Pulse Reject
JP2 = A,B,C,D, SHORT
JP3 = 2048
JP4 = 8 Bit
JP5 = OPEN
JP6 = SHORT

WAVEFORM VARIABLES

TD > 2 us
TPW = 50 ± 5 ms
~98% duty cycle
VCCP = 5.0 ± .25 V.
VPP = 25.0 ± 1.0 V.

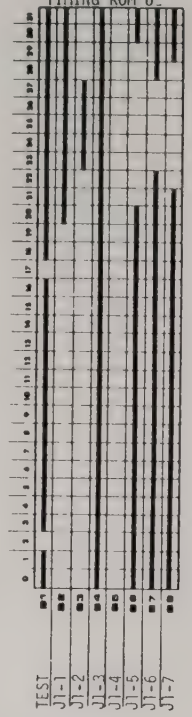
For calibration, the card set polarity defaults to VOL.

○ These waveforms correspond to callouts on the Calibration Chart. Switch S2 and S3 of the Universal Calibrator to indicated positions to obtain waveforms. Refer to Performance Check section of manual for detailed steps.

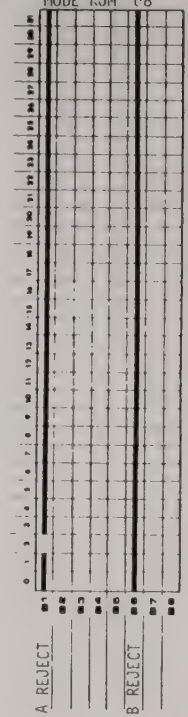
TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)

TIMING ROM U2



MODE ROM U8



DATA I/O ISSAQUAH, WASH.

INTEL , T.I. SINGLE VOLTAGE MOS	DRAWN BY: K. LANZ APPROVED BY:
TITLE: TIMING DIAGRAM	
DATE: 6-2-78	DRAWING NUMBER: 007-1512

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5: Observe the START and STOP indicators.

Model 9: Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.

System 19: Observe the START light.

4.3.2 SET THE STATE OF THE START/STOP LINE

To set the state of the START/STOP line:

Models 1, 2, 3 and 5: Press the START/STOP key.

Model 9: Press KEYBOARD to STOP; press EXECUTE to START.

System 19: To set the START line high, with KEYBD selected and address and data displayed, depress the START key. Reselect KEYBD to STOP.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5: Press the FWD key or the REV key.

Model 9: See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.

Revision "A" Software: Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify:

1. Ground J1-16 on the analog card.
2. Press LOAD.
3. Press EXECUTE.
4. Press KEYBOARD.
5. Key in data – Ø1 hex – at address ØØ1.
6. Press VERIFY.
7. Press EXECUTE. The programmer will mis-verify at the address containing data and will STOP in FWD.
8. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software: Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19: With KEYBD selected, press ENTER to set the programmer in FORWARD and REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the calibration chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5: Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3: Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9: (See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.) When using a Model 9, always key in the hex data in parentheses to be sure that the correct data is placed on the DI bus.

Revision "A" Software:

Halt the programmer in the automatic program mode with data on the DI bus.

1. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.
2. Press the KEYBOARD key, and key in hex data called out in parentheses on the calibration chart.
3. Press the PROGRAM key.
4. Ground J1-16 on the analog card.
5. Press EXECUTE and wait for the programmer to abort.
6. Press STOP, KEYBOARD and EXECUTE.
7. Disconnect J1-16 from ground.
8. SET the address specified on the calibration chart in order to make the measurement.

Revision "B" or later Software:

1. With the EXECUTE indicator illuminated and all the others OFF, use the hex keypad to key in hex data called out in parentheses on the calibration chart.

System 19:

Key the hex data in parentheses into RAM at the specified address. The data and address shown in the display are present on the DI bus.

4.3.5 CONFIRM DATA ON THE DO BUS

To view DO Bus data:

Models 1, 2, 3 and 5: Compare the bit callout on the calibration chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF.

Model 9: Press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the calibration chart.

System 19: With KEYBD selected, press the DEVICE DATA key.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the timing diagram, are indentically referenced on the Calibration Chart. Waveforms are selected using switches S2 and S3 on the Universal Calibrator as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

1. Make sure that the programmer power is OFF.
2. Remove the digital card from the card slot.
3. Check the timing diagram to determine the number of the reject jumper. Find and remove the jumper on the digital card (if installed), making sure to note the position in which it is installed.

CAUTION

Be sure to replace the reject (abort) jumper (if it was installed) in the proper position after waveform observation.

4. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.
5. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.
6. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point as indicated to the left of the TEST waveform on the timing diagram. Connect an input probe to TP3 on the calibrator.
7. Reinstall the digital card in the slot from which it was removed.

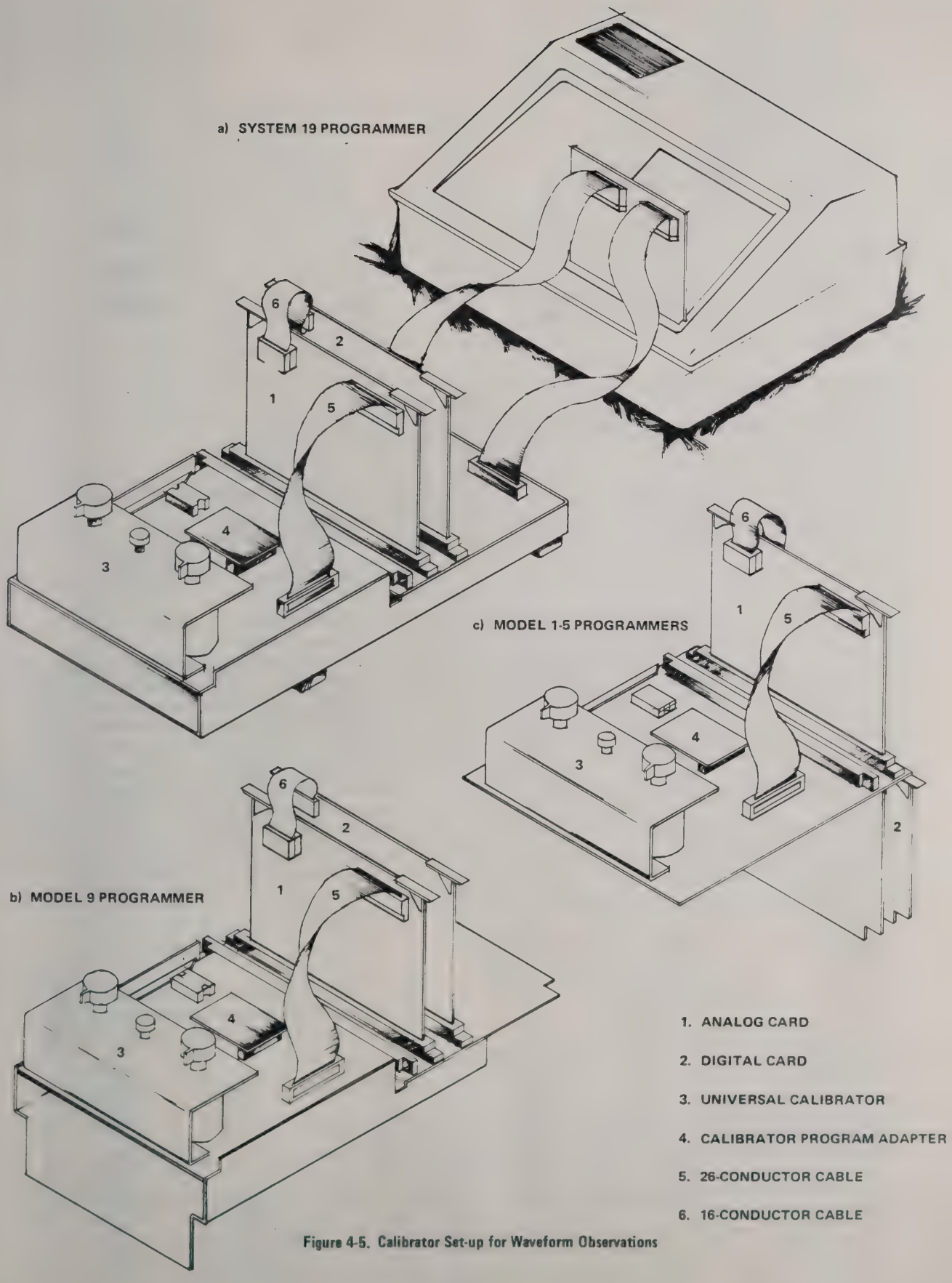


Figure 4-5. Calibrator Set-up for Waveform Observations

8. Check the NOTES column of the timing diagram to determine whether the Program Card Set defaults to VOH or VOL for calibration. If and only if the card set defaults to VOH, ground J1-16 (Read Enable line) to the GND test point on the Universal Calibrator.

CAUTION

Do not connect J1-16 to any other potential; damage to programmer components may result.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.

2. Prepare the programmer for keyboard data entry.

Models 1 – 5, press:	RESET RAM-RAM PROGRAM MANUAL START
Model 9:	Set the NORMAL/INVERT switch in NORMAL if the Program Card Set is calibrated VOH or in the INVERT position if VOL. The NOTES column on the timing diagram specifies the correct polarity. Press: KEYBOARD.
System 19 press:	KEYBD Ø ENTER

3. Key in data for bit 1 at several addresses:

Models 1 – 5:	Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display.
Model 9:	Enter hex data "Ø1" at several addresses.
System 19:	Enter hex data at several addresses. Check the NOTES column on the Timing Diagram to determine the correct data polarity. If the timing diagram indicates VOH, enter a hex "1". If the timing diagram indicates VOL, enter a hex "E" for 4-bit card sets; "FE" for 8-bit card sets.

4. Select the PROGRAM mode:

Models 1 – 5, press:	RESET PROGRAM AUTO RAM-ROM2
Model 9, press:	PROGRAM
System 19, press:	SELECT CØ START PROG

5. Initiate waveforms:

Models 1 – 5, press:	START
Model 9, press:	EXECUTE
System 19, press:	START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the timing diagram and calibration chart by the circled digits (①, ②, ③,...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the calibration charts is of no importance during waveform observation.

CAUTION

When S1 is depressed high currents are induced within the programmer; do not hold S1 depressed for extended periods.

6. Stop programming:

Models 1 – 5 and 9, Press:	STOP
System 19, press:	KEYBD

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

CALIBRATION CHART 017-1512 — PROGRAM CARD 909-1512

FIXTURE 702-1071 — MANUFACTURER INTEL, T.I.

PROGRAM ADAPTER 910-1512 — PROM Single Voltage MOS

DATE	REV	REVISION RECORD	DR	CK
6-2-78	A	RELEASE	DB	
11-78	-	ECN #2565	FS	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U2.	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
44	00	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5
44	00	POWER +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8
44	00	SUPPLIES +5	1-3	000	00	000			+5	R18	5.05	5.1	5.15
44	00	-9	1-4	000	00	000			-9	R40	-9.2	-9.0	-8.8
44	00	PROGRAMMABLE SUPPLY	1-5	000	00	000			PROG V		11.0		14.0
44	00	VCC PROGRAM (1)	2-1	001	01	001	5	1	TP3	R6	4.75	5.00	5.25
44	00	VCC CURRENT LIMIT	2-2	001	01	001	6	1	TP3		-0.05		0.4
44	00	COMPARATOR REFERENCE	3-1	001	01	001			U5 P8		1.4		1.8
44	00	$\overline{CE}$ PROGRAM (2)	4-1	002	02	002	7	5	TP3		4.75		5.25
44	01	$\overline{CE}$ VERIFY	4-2	003	03	003	7	5	TP3		0.0		0.4
44	30	VPP PROGRAM (3)	4-3	004	04	004	3	6	TP3	R9	24.0	25.0	26.0
44	30	VPP CURRENT LIMIT	4-4	004	04	004	5	6	TP3		-0.05		0.4
44	30		4-5	004	04	004							
44	00	VPP VERIFY	4-6	005	05	005	3	6	TP3		4.75		5.25
44	00	PD/$\overline{PGM}$ PROGRAM (6)	4-7	006	06	006	7	7	TP3		4.75		5.25
44	02	PD/$\overline{PGM}$ VERIFY	4-8	007	07	007	7	7	TP3		0.0		0.4
C4	00	BIT 8 PROGRAM	5-1	008	08	010	2	8	TP3		-0.05		0.4
C4	00	BIT 7 PROGRAM	5-2	008	08	010	2	9	TP3		2.3		2.7
C4	00	BIT 6 PROGRAM	5-3	008	08	010	2	10	TP3		-0.05		0.4
C4	00	BIT 5 NO PROGRAM	5-4	008	08	010	2	11	TP3		2.3		2.7
C4	00	BIT 4 PROGRAM	5-5	008	08	010	2	12	TP3		-0.05		0.4
C4	00	BIT 3 NO PROGRAM	5-6	008	08	010	2	23	TP3		2.3		2.7
C4	00	BIT 2 PROGRAM	5-7	008	08	010	2	22	TP3		-0.05		0.4
C4	00	BIT 1 NO PROGRAM	5-8	008	08	010	2	21	TP3		2.3		2.7
C4	00	BIT 8 NO PROGRAM	5-9	008	08	010	2	8	TP3		2.3		2.7
C4	00	BIT 7 PROGRAM	5-10	008	08	010	2	9	TP3		-0.05		0.4
C4	00	BIT 6 NO PROGRAM	5-11	008	08	010	2	10	TP3		2.3		2.7
C4	00	BIT 5 PROGRAM	5-12	008	08	010	2	11	TP3		-0.05		0.4
C4	00	BIT 4 NO PROGRAM	5-13	008	08	010	2	12	TP3		2.3		2.7

COMMENTS

Switch S1 must be depressed for accurate readings.
CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

Adjustments are located on the power supply board. See programmer manual. See NOTE 1.

Adjustment Step. Confirm programmer in STOP. Test point located on analog card.

Confirm programmer in STOP.

Load bits 2, 4, 6 & 8 ON (HEX AA) to DI Bus.

Confirm bits 2, 4, 6 & 8 ON (HEX 55) on DO Bus.

Load bits 1, 3, 5 & 7 ON (HEX 55) to DI Bus.

Confirm bits 1, 3, 5 & 7 ON (HEX AA) on DO Bus.

CAL. ADAPT HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
C4	00	BIT 3 PROGRAM	5-14	008	08	010	2	23	TP3		-0.05		0.4
C4	00	BIT 2 NO PROGRAM (5)	5-15	008	08	010	2	22	TP3		2.3		2.7
C4	00	BIT 1 PROGRAM (4)	5-16	008	08	010	2	21	TP3		-0.05		0.4
C4	40	DATA DISABLE	5-17	009	09	011							
44	00	ADDRESS TEST VIL (7)	6-1	682	2AA	1252	7	20	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-2	682	2AA	1252	7	19	TP3		4.8		5.15
44	00	ADDRESS TEST VIL	6-3	682	2AA	1252	7	18	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-4	682	2AA	1252	7	17	TP3		4.8		5.15
44	00	ADDRESS TEST VIL	6-5	682	2AA	1252	7	16	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-6	682	2AA	1252	7	15	TP3		4.8		5.15
44	00	ADDRESS TEST VIL	6-7	682	2AA	1252	7	14	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-8	682	2AA	1252	7	13	TP3		4.8		5.15
44	00	ADDRESS TEST VIL	6-10	682	2AA	1252	7	2	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-11	682	2AA	1252	7	3	TP3		4.75		5.15
44	00	ADDRESS TEST VIL	6-12	682	2AA	1252	7	4	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-13	1365	555	2525	7	20	TP3		4.75		5.15
44	00	ADDRESS TEST VIL	6-14	1365	555	2525	7	19	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-15	1365	555	2525	7	18	TP3		4.75		5.15
44	00	ADDRESS TEST VIL	6-16	1365	555	2525	7	17	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-17	1365	555	2525	7	16	TP3		4.75		5.15
44	00	ADDRESS TEST VIL	6-18	1365	555	2525	7	15	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-19	1365	555	2525	7	14	TP3		4.75		5.15
44	00	ADDRESS TEST VIL	6-20	1365	555	2525	7	13	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-21	1365	555	2525	7	2	TP3		4.75		5.15
44	00	ADDRESS TEST VIL	6-22	1365	555	2525	7	3	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	6-23	1365	555	2525	7	4	TP3		4.75		5.15
44	00	GROUND TEST	7-1	1365	555	2525	8	24	TP3		0.0		0.08
44	00	ALL TEST VIL	8-1	2047	7FF	3777			R50		0.0		0.4
44	00	ALL TEST VIH	8-2	2048	800	4000			R50		4.75		5.15
44	00	4K GATE TEST	9-1	000	00	000							
44	00	←——DATA PATTERN FOR ALL WORDS NOT SHOWN											

CALIBRATION CHART 017-1512

PAGE 2 OF 2

Load bits 1,3,5 & & ON (Hex 55) to DI bus.
Confirm bits 1,3,5 & & ON (Hex AA) on DO bus.

Model 5: Load bits 1,3,5,7 ON to DI bus.
All programmers: Confirm all bits OFF (Hex FF) on DO bus.

Test Point: Top of R50 on analog card. See NOTES 2 and 3.

NOTES:
1. For the System 19, the limits of this supply are 0.1 volt less than specified.
2. Omit these tests when using programmers with less than 4K of RAM.
3. Models 1-5: 1) Press the STOP key; 2) Ground the TOP of R45 on the analog card; 3) Confirm bit 7 ON on DO Bus.
   Model 9: 1) Press the KEYBOARD key; 2) Hold SET depressed and enter FFF on keyboard; 3) Release SET; 4) Confirm FFF in Address Display.

NOTES (cont'd.):
System 19: 1) Press KEYBOARD; 2) Enter FFF on keyboard; 3) Confirm FFF in Address Display.

4.4.3 REJECT JUMPER REINSTALLATION AND ABORT TEST

Before putting the Program Card Set back in use, it is necessary to reinstall the reject (abort) jumper and confirm the operation of the abort function on the digital card.

1. Turn the programmer power OFF.
2. Remove the digital card from the card slot.
3. Refer to the Timing Diagram for the reject jumper number and make sure to install the jumper in the position from which it was removed.
4. Reinstall the digital card in the card slot.
5. Repeat the key sequence in Waveform Test Procedure, paragraph 4.4.2, steps 1-5.
6. With Universal Calibrator switch positions selected to observe the test pulse waveform, repeat step 6 of the Test Procedure. Note with the oscilloscope that the waveform display is terminated by the programmer. This indicates that the abort function of the digital card is operative.

SECTION 5
CIRCUIT DESCRIPTION

5.1 INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 5-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

5.1.1 DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signalled or until the bit is programmed.

5.1.2 ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturers' specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow, timing and reject conditions. Detailed circuit schematics are found at the rear of this manual – refer to these for pin-out and interconnection information.

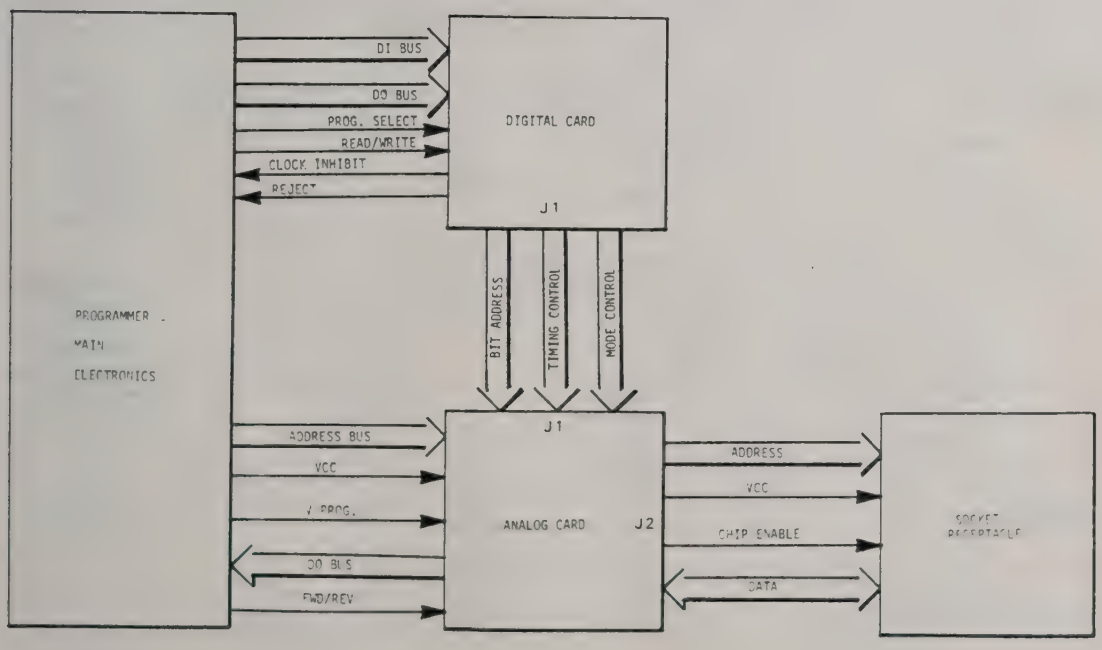


Figure 5-1. Simplified Block Diagram of Program Card Set

5.2 DIGITAL CARD

5.2.1 BLOCK DIAGRAM

Figure 5-2 gives a generalized block diagram of the digital card. This diagram shows signal flow and functional relationships between the blocks, but does not include detailed interconnection information. Refer to the schematics and Timing Diagram (with truth tables) for details of circuit connection and operation. The following paragraphs discuss the functions performed by the digital card.

5.2.2 SELECT AND MODE CONTROL

The select gates monitor status lines on the programmer MEU. When the digital card is selected for operation the status lines are enabled. Selection Gate output enables the digital card and pulls CLK INH (MEU) to signal the programmer to recognize the digital card. Prior to selection, the master clock is stopped and all counters and memories are initialized.

5.2.3 MASTER CLOCK

Upon selection of the digital card, the Master Clock is enabled and runs free at the frequency set by R3, R4, and C9. This clock drives the sequence counter, which addresses the Timing ROM. A clock rate output from the Timing ROM enables two-speed clock operation.

5.2.4 TIMING GENERATOR

The Timing Generator consists of a 4-bit sequence counter addressing a 32x8 Timing ROM. This combination generates timing signals for analog card control to provide the dynamic waveforms presented to the PROM during Program and Read. This generator also outputs clock rate and provides the test pulse. The test pulse is used on the digital card to enable testing of the PROM outputs during the Read portion of the programming cycle.

5.2.5 READ OPERATION

The Bit Comparator compares the DI and DO bus and outputs to the bit-to-program control gating. When Test and the Comparator output yield no bit to program, the Program Pulse Counter outputs a borrow pulse. This pulse stops the Master Clock and releases the CLK INH line. The release of CLK INH signals the programmer to deselect the digital card. With the digital card deselected, the programmer advances the word count and reselects the digital card.

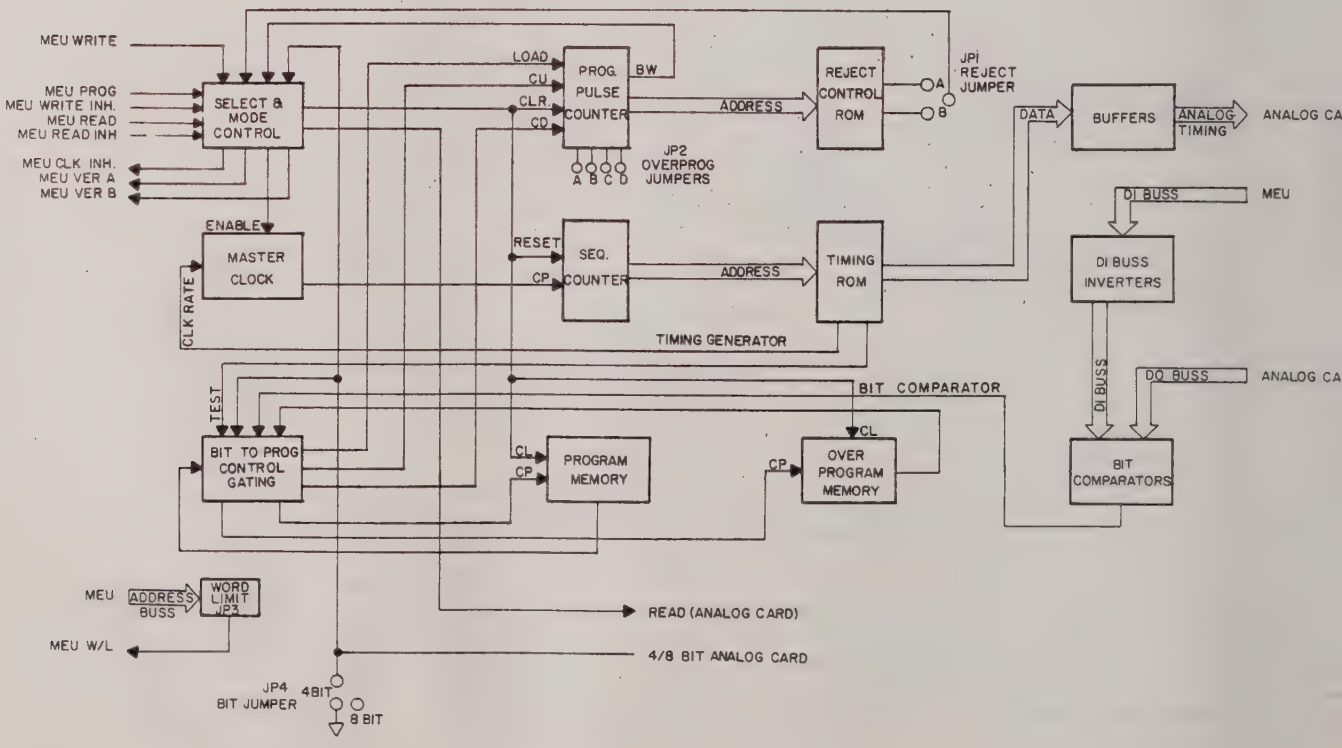


Figure 5-2. Block Diagram, 1348 Digital Program Card

5.2.6 PROGRAM OPERATION

When Test and the Comparator output yield a bit to program, the Program Memory sets and the Program Pulse Counter advances. The Timing Generator outputs program pulse waveforms to the analog card and loops back to Test. This sequence repeats until Test yields that the PROM bits have programmed (no bit to program), or until the Program Pulse Counter counts the maximum number of allowed program pulse attempts. This counter advances following each program pulse and addresses the Reject Control ROM. When the Counter reaches its reject count as determined by the Reject Control ROM and jumper JP1, a reject is signaled.

5.2.7 OVERPROGRAM OPERATION

With the Program Memory set (program operation in progress) and Test indicating no bit to program (PROM bits have programmed), the Program Pulse Counter loads to the binary value of the JP2 overprogram jumpers.

Loading of this counter is enabled only when the Program Memory is set. This prevents the digital card from applying any program pulses to PROM bits that were already programmed when first read. Following loading of this counter, the Overprogram Memory sets, releasing load and enabling countdown on the Program Pulse Counter. A program pulse is outputted from each countdown. When count Ø is reached, borrow from this counter stops the Master Clock and releases CLK INH. The release of CLK INH signals the programmer to deselect the digital card. With the digital card deselected, the programmer advances the word count and the entire sequence is repeated for the next word.

5.2.8 WORD LIMIT

Word Limit value is jumper-selected by JP3. This value limits the address range of the programmer through the Word Limit pin on the MEU.

5.2.9 4/8 BIT MODE

The digital card is selected for either 4- or 8-bit-wide operation by the 4/8 bit line. This line is enabled by either JP4 or the socket adapter being used. When this line is low, the four high-order bits (bits 5 through 8) and VER. 8 are disabled. By this means the digital card and programmer are matched to the bit width of the PROM being programmed.

5.3 ANALOG CARD

5.3.1 BLOCK DIAGRAM

Figure 5-3 shows a block diagram of the analog card. This diagram shows signal flow and functional relationships between the blocks, but does not include detailed interconnection information. Refer to the schematics and timing diagram (with truth tables) for

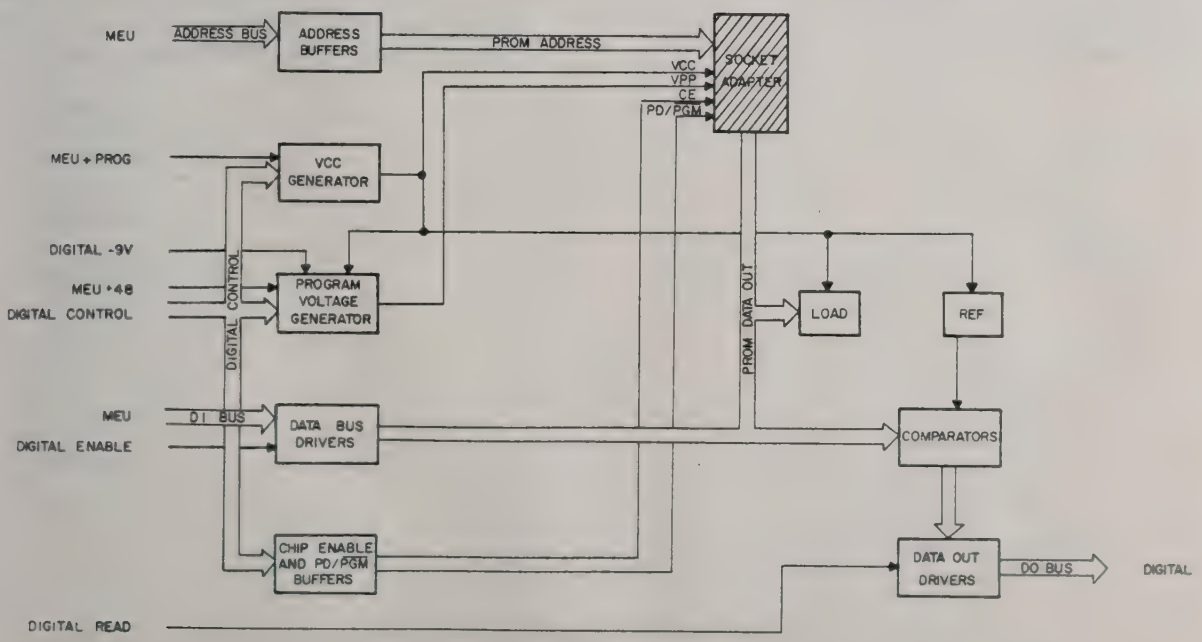


Figure 5-3. Block Diagram, 1512 Analog Card

details of circuit connection and operation. The following paragraphs discuss the functions performed by the analog card.

Address buffers accommodate the ten incoming address lines emanating from the programmer MEU. The buffers consist of noninverting gates with uncommitted collector outputs. Buffer outputs have resistor pull-ups to PROM VCC.

5.3.2 VCC GENERATOR

The VCC generator consists of a common emitter amplifier (Q1) controlled by a differential amplifier (Q2 and Q3). R6 provides a feedback path to the amplifier and serves as output voltage adjustment. The reference for the differential amplifier is determined by adjustable shunt regulator (Q10) and voltage divider action of R30, R37 and R19.

The generator output is held to zero volts when the programmer is in Stop. Fold-back current limiting is accomplished via Q6, Q14 and Q15. When excess VCC current is drawn, Q14 turns on, turning on Q6 and Q15. Q6 holds the shunt regulator output (differential reference) to 0 volts, thereby holding VCC to 0 volts. Q15 pulls Reset, Reset pulls Stop, and Stop holds the reference to 0 volts.

5.3.3 PROGRAM VOLTAGE GENERATOR (VPP)

The Program Voltage Generator consists of transistors Q7 and Q12 driven by Q8 and Q9 and controlled by the differential amplifier Q4 and Q5. The output is push-pull with active pull-up and pull-down. The pull-up transistor is tied to either +Program or +48 by jumper JP5. The pull-down transistor is tied to -9V, or ground by jumper JP4.

The reference voltage for the differential amplifier is VCC. R15 provides the negative feedback path. The output voltage is adjusted by R9 via JP3. R9 is jumpered to JP-5 by JP1. When J1-5 is low, the generator output sets at the value of VCC. When J1-5 is high, the output can be adjusted above VCC to a higher positive value. Foldback current limiting is present on both the pull-up and pull-down source. The output is held to 0 volts when the programmer is in Stop.

5.3.4 DATA BUS DRIVERS

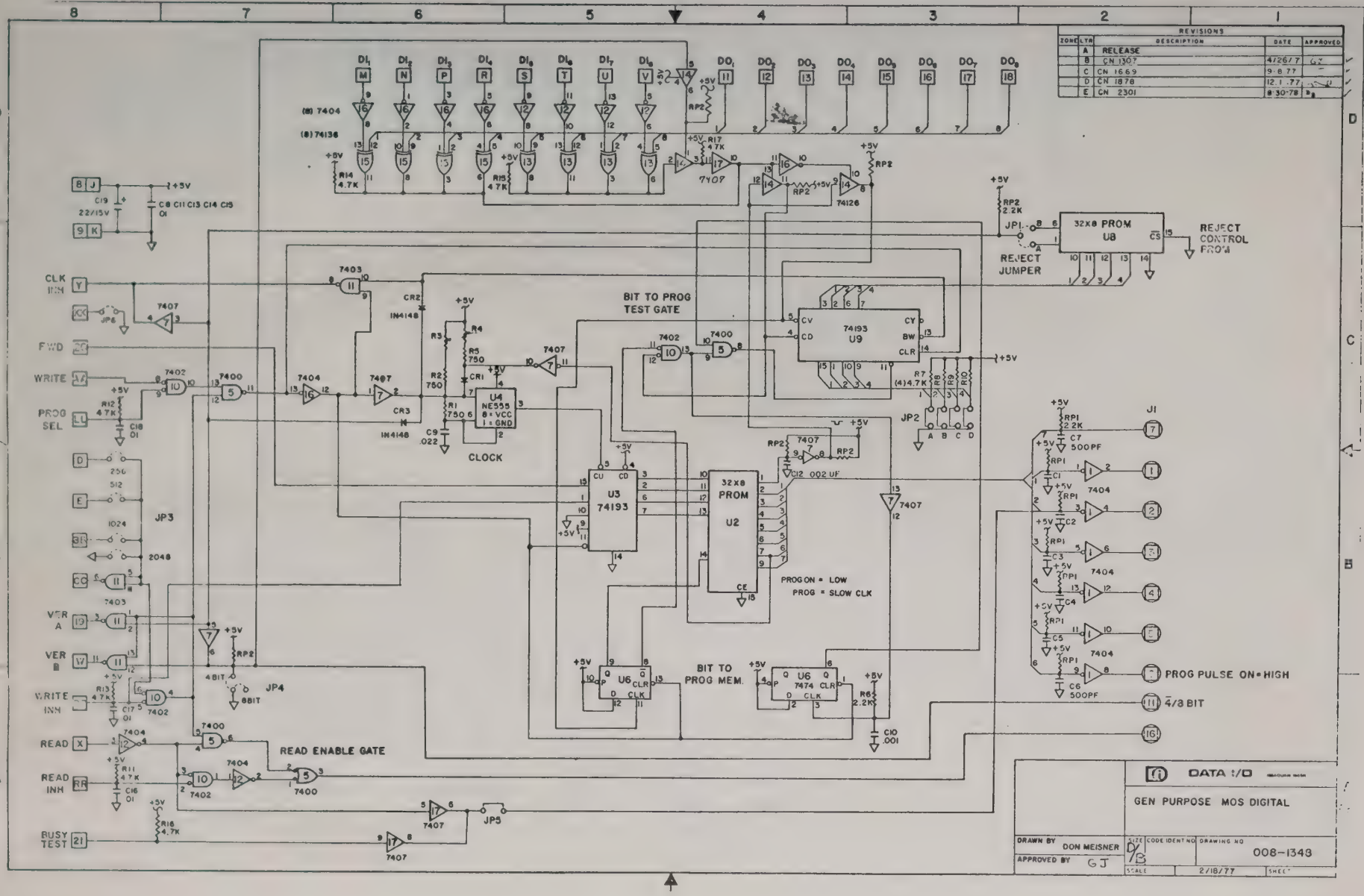
Data from the DI Bus is presented to Gates U2, U3, U6 and U7. Outputs from these gates drive the PROM bits during program. During Read, Data Enable disables the gate outputs and data from the PROM is presented to the comparator.

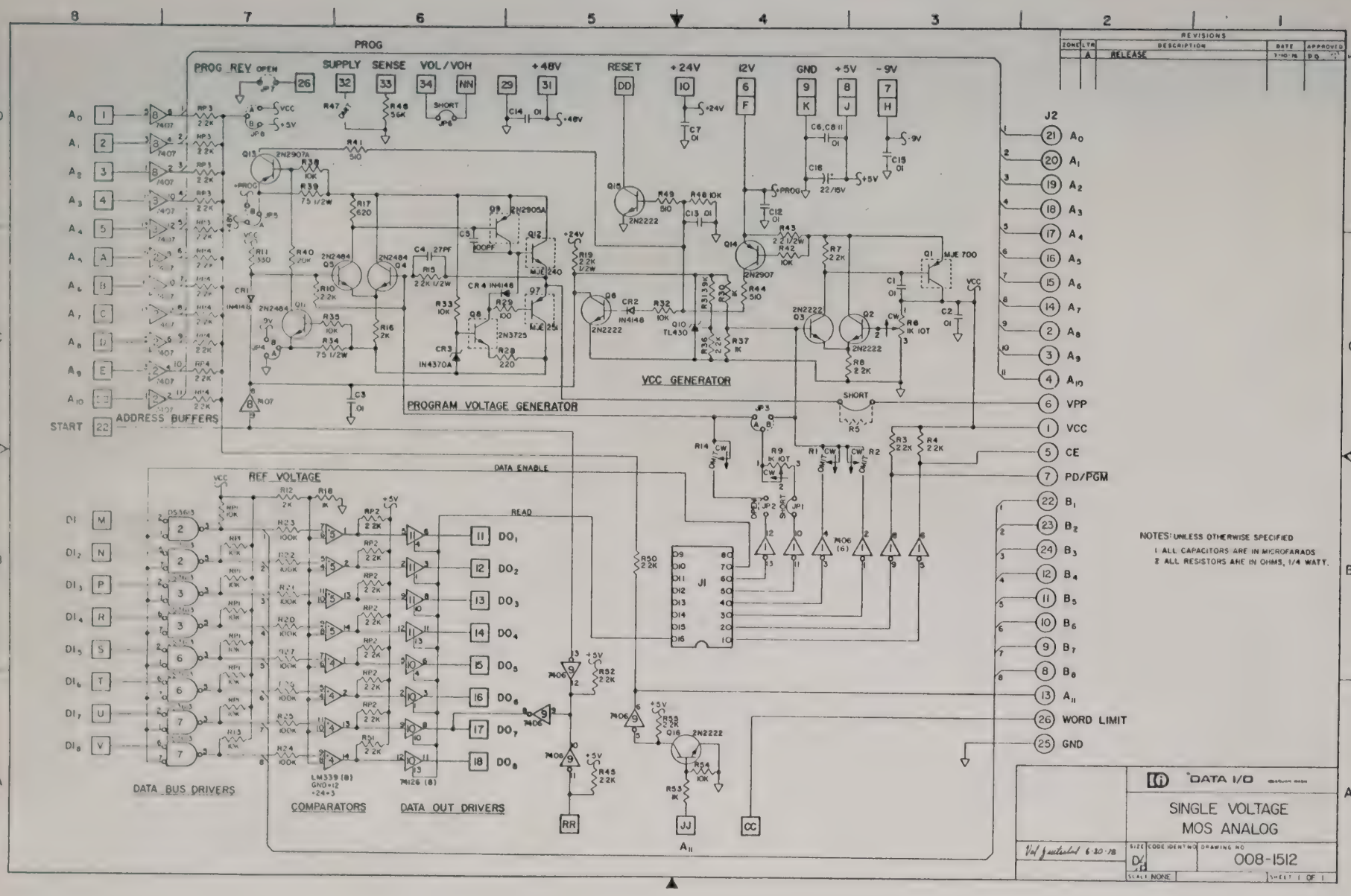
5.3.5 COMPARATOR AND DATA OUT DRIVERS

The comparator compares PROM bit data against the reference level. The reference for the comparator is determined by voltage divider R12 and R18. Comparator outputs are transferred to the DO Bus during Read by the data out drivers. This transfer allows the digital card to make a digital comparison of the transferred PROM output (DO Bus) to the programmer DI Bus.

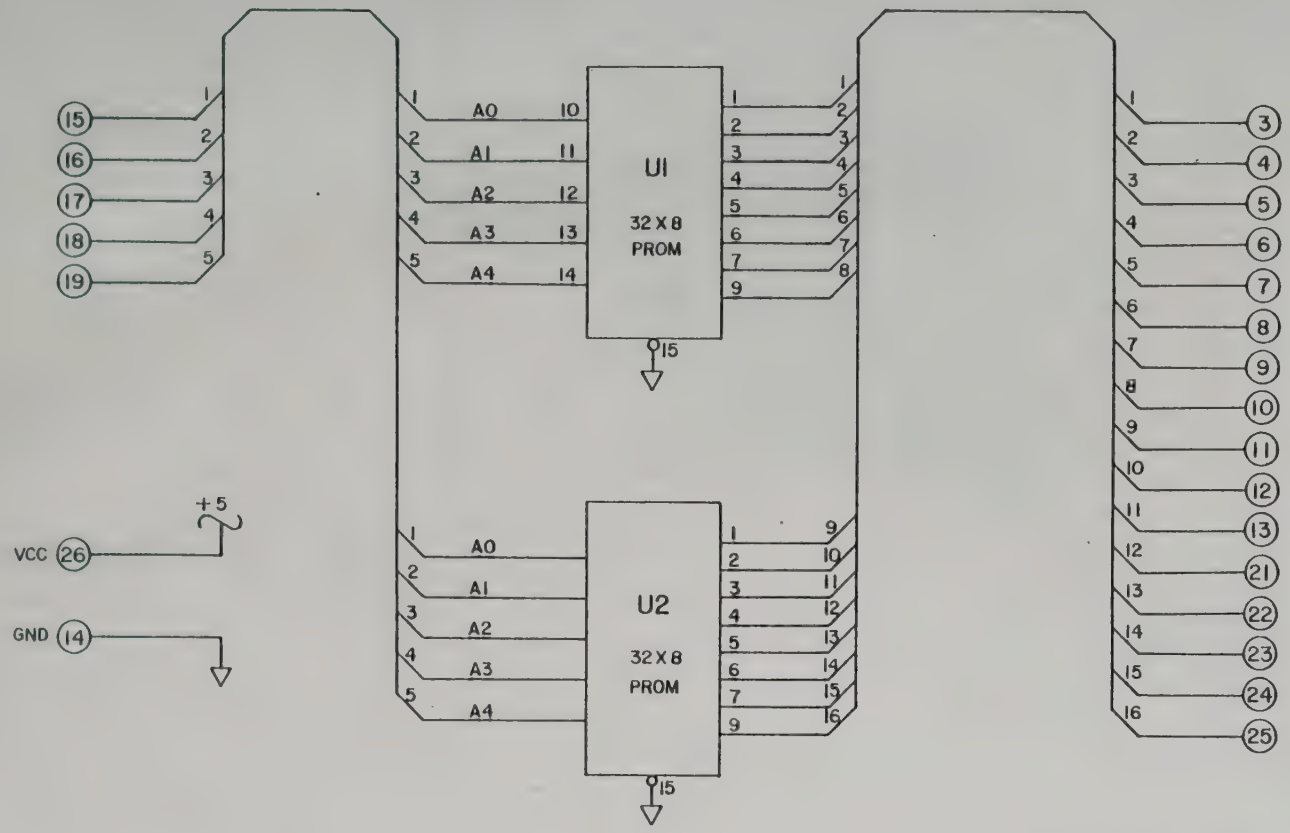
5.3.6 CHIP ENABLE AND PD/PGM BUFFERS

These buffers output the specified CE and PD/PGM voltage levels to the PROM during Program and Read. Their outputs are resistively pulled up to the VCC supply.


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A RELEASE
B CN 1307 4/26/77
C CN 1669 9-8-77
D CN 1878 12-1-77
E CN 2301 8-30-78
(8) 7404
(8) 74136
7407
74126
RP2
RP2 2.2K
32X8 PROM U8
JP1
REJECT JUMPER
REJECT CONTROL FROM
CLK IN
FWD
WRITE
PROG SEL
7403
7407
7402
7400
7404
CR2 IN4148
CR3 IN4148
BIT TO PROG TEST GATE
74193 U9
JP2
U4 NE555 8=VCC 1=GND
CLOCK
U3 74193
32X8 PROM U2
PROG ON = LOW
PROG = SLOW CLK
JP3
256
512
1024
2048
VER A
VER B
WRITE INH
4 BIT
8 BIT
JP4
READ
READ INH
READ ENABLE GATE
BUSY TEST
JP5
BIT TO PROG MEM.
U6 7474 CLR
J1
PROG PULSE ON=HIGH
4/8 BIT
DATA I/O
GEN PURPOSE MOS DIGITAL
DRAWN BY DON MEISNER
APPROVED BY GJ
SIZE B
CODE IDENT NO
DRAWING NO 008-1348
SCALE
2/18/77
SHEET


PROG
PROG REV OPEN
SUPPLY SENSE
VOL/VOH
+48V
RESET
+24V
12V
GND
+5V
-9V
ADDRESS BUFFERS
START
PROGRAM VOLTAGE GENERATOR
VCC GENERATOR
REF VOLTAGE
DATA ENABLE
READ
DATA BUS DRIVERS
COMPARATORS
DATA OUT DRIVERS
J2
VPP
VCC
CE
PD/PGM
WORD LIMIT
GND
NOTES: UNLESS OTHERWISE SPECIFIED
1 ALL CAPACITORS ARE IN MICROFARADS
2 ALL RESISTORS ARE IN OHMS, 1/4 WATT.
DATA I/O
SINGLE VOLTAGE
MOS ANALOG
008-1512
Val Justeland 6-20-78

DATE	SYM	REVISION RECORD	DR	CK
11-13-75	A	RELEASE		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH		
DECIMAL .		SCALE	DRAWN BY G. ROPPE
FRACTIONAL .	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		APPROVED BY
ANGULAR .	DATE 10-15-75	DRAWING NUMBER 008-1072	

808

DATA I/O

Programming systems for tomorrow...today

Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual: _____

How can this manual be improved: _____

_____

_____

Additional comments: _____

_____

Name _____

Company _____ Department _____ M/S _____

Address _____

City _____ State _____ Zip _____ Phone _____

Manual or Part No. _____

Warranty/Registration

Please return this card to Data I/O within five days

Did the packaging of this equipment exhibit any outward signs of physical damage? . . . . . YES ○ ○ NO
Did this equipment arrive intact, without loose parts or cable damage? . . . . . YES ○ ○ NO
Did the equipment operate on power-up?. . . . . YES ○ ○ NO
Did you attain adequate system performance? . . . . . YES ○ ○ NO
Were any electrical adjustments required? . . . . . YES ○ ○ NO
If you required assistance, was a local Data I/O representative contacted? . . . . . YES ○ ○ NO

Comments – _____

_____

Name _____ Title _____

Department _____ M/S _____

Company _____

Address _____

City _____ State _____ Zip _____ Phone ( ) _____

Model or Description _____ Serial or Part No. _____

Date Received _____

90 Day Warranty

Data I/O warrants that all equipment sold pursuant to any resultant agreement shall be free from defects in material or workmanship at the time of delivery. Such warranty shall extend for 90 days. Buyer must provide notice to Data I/O within this prescribed warranty period of any defect; if the defect is not the result of improper usage, service, maintenance or installation and equipment has not been otherwise damaged or modified after delivery, Data I/O shall either replace or repair the defective part or parts of equipment or replace the equipment or refund the purchase price at Data I/O's option after return of such equipment by buyer to Data I/O. Shipment to and from Data I/O's facility shall be borne on account of buyer.

(a) Consequential Damages — Data I/O shall not be liable for any incidental or consequential damages incurred as a result of any defect in any equipment sold hereunder and Data I/O's liability is specifically limited to its obligation described herein to repair or replace a defective part or parts covered by this warranty.

(b) Exclusive Warranty — The warranty set forth herein is the only warranty, oral or written made by Data I/O and is in lieu of and replaces all other warranties, expressed or implied, including the WARRANTY OF MERCANTIBILITY AND THE WARRANTY OF FITNESS FOR PARTICULAR PURPOSE.

DATA I/O
Programming systems for tomorrow...today

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL FIRST CLASS Permit No. 24 Issaquah, WA 98027

Postage will be paid by:

DATA I/O Reader Comments

Director of Sales Support
P. O. Box 308
1297 Northwest Mall
Issaquah, WA 98027

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL FIRST CLASS Permit No. 24 Issaquah, WA 98027

Postage will be paid by:

DATA I/O Warranty/Registration

Service Manager
P. O. Box 308
1297 Northwest Mall
Issaquah, WA 98027

DATA I/O

Programming systems for tomorrow...today